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Sheet 1

of 1

Application Number	10/734,627
Filing Date	12/12/2003
First Named Inventor	J. Bharadwaj
Art Unit	2186 2181
Examiner Name	Not yet assigned Jesse Moll
Attorney Docket Number	P17845

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/JM/	1	S. Pinter, "Register Allocation with Instruction Scheduling: a New Approach", Dept. of Electrical Engineering, Israel Institute of Technology, Haifa, Israel, 19 pages. June 1993	
/JM/	2	D. Bradlee et al., "Integrating Register Allocation and Instruction Scheduling for RISCs", Dept. of Computer Science, Univ. of Washington, Seattle, Washington, 1991, 9 pages.	
/JM/	3	G. Chaitin, "Register Allocation & Spilling Via Graph Coloring", IBM Research, Yorktown Heights, NY, 1982, 4 pages.	
/JM/	4	M. Poletto et al., "Linear Scan Register Allocation" ACM Trans. on Programming Languages and Systems, Vol. 21, No. 5, Sept. 1999, Pages 895-913.	
/JM/	5	S. Freudenberger et al., "Phase Ordering of Register Allocation and Instruction Scheduling", Presented at Code Generation - Concepts, Tools & Techniques, July 1991, 10 pages.	
/JM/	6	F. Chow et al., "The Priority-Based Coloring Approach to Register Allocation", ACM Trans. on Programming Languages and Systems, Vol. 12, No 4, October 1990, pages 501-536.	

Examiner Signature	/Jesse Moll/	Date Considered	09/29/2008
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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